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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER	
GEBRESILASSIE, KIBROM K	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amended application filed on October 30, 2006.

2. Claims 1-6, and 8-11 are pending.

3. Claim 7 is canceled.

4. Claims 1, 4, 6, 8, 10, and 11 are amended.

Response to Arguments

5. Regarding applicants response to Drawing objection: Applicants are replaced an objected drawings with a corrected drawing sheets to overcome the objection made in previous Office action. Accordingly, the objection is withdrawn.

6. Regarding applicants response to 102 and 103 rejection: Applicant's arguments with respect to the rejection(s) of claim(s) 1-11 under 102(b) and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hill et al and Dane et al.

7. Regarding applicants response to 101 rejection: Examiner appreciates applicants for amending the claims in order to overcome the 101 rejection. However, the amended claim could not overcome the rejection [See Claim rejection under 35 USC § 101 below]. Accordingly, the rejection is maintained.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. The claimed invention of claims 6, 10, and 11 do not appear to recite a tangible result. Data transformation is not the same as physical transformation. The tangible requirement does require that the claim must recite more than a 35 U.S.C. 101 judicial exception, in that the process claim must set forth a practical application of that judicial exception to produce a real-world result. The claimed elements in this case, are simply a thought or computation element, and without having a tangible result. It is not until the transformation applied in a meaningful way that it has a real world value and becomes a tangible result.

MPEP 2106 states as follows:

"The tangible requirement does not necessarily mean that a claim must either be tied to a particular machine or apparatus or must operate to change articles or materials to a different state or thing. However, the tangible requirement does require that the claim must recite more than a 35 U.S.C. 101 judicial exception, in that the process claim must set forth a practical application of that judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 (invention ineligible because had "no substantial practical application."). "[A]n application of a law of nature or mathematical formula to a ... process may well be deserving of patent protection." Diehr, 450 U.S. at 187, 209 USPQ at 8 (emphasis added); see also Corning, 56 U.S. (15 How.) at 268, 14 L.Ed. 683 ("It is for the discovery or invention of some practical method or means of producing a beneficial result or effect, that a patent is granted . . ."). In other words, the opposite meaning of "tangible" is "abstract."

b. Claims 1, and 4 are rejected under 35 U.S.C. 101 because "first circuitry" and "second circuitry" are just software per se that resides in a memory (See: Specification Page 8 lines 10-18 and [0026]). Because the claimed invention of Claims 1, and 4 are system claims, the claims should have associated with hardware such as "processor" or "memory" in the body of the claim in order to be statutory. Accordingly, Claims 1, and 4 are rejected being non-statutory.

MPEP 2106 states as follows:

" computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Accordingly, it is important to distinguish claims that define descriptive material per se from claims that define statutory inventions."

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by US. Patent No. 6,298,452 issued to Hill et al.

As per Claim 1:

Hill discloses a hardware emulator for verifying a plurality of systems on a plurality of chips (See: Col. 3 lines 51-59, Col. 5 lines 3-8; Fig. 1), said emulator comprising:

a first circuitry (such as *emulator of hardware Model B*; See: Fig. 1) for verifying a first system on a chip; and a second circuitry (such as *emulator of Hardware Model C;* See: Fig. 1) for verifying a second system on another chip while verifying the first system on chip (See: Abstract lines 5-8, Col. 5 lines 24-26 and 31-33; Fig. 1).

As per Claim 2:

Hill discloses the hardware emulator of claim 1, further comprising: a first interface for providing inputs to the first circuitry and receiving outputs from the first circuitry; and a second interface for providing inputs to the second circuitry and receiving outputs from the second circuitry (such as *signal Bus 1 and Signal Bus 2*; See: Fig. 1, Fig. 3).

As per Claim 3:

Hill discloses the hardware emulator of claim 1, wherein the first circuitry is configured to realize the first system on a chip; and the second circuitry is configured to realize the second system on another chip (See: Col. 8 lines 35-37).

As per Claim 4:

Hill discloses a hardware emulator for verifying a plurality of systems on a plurality of chips (See: Col. 5 lines 3-8; Fig. 1), said emulator comprising: a first circuitry configured to realize a first system on a chip; and a second circuitry configured to realize a second system on chip while verifying the first system on another chip (See: Col. 8 lines 35-37), the second circuitry connected to the first circuitry (See: Col. 5 lines 46-48).

As per Claim 5:

Hill discloses the hardware emulator of claim 4, further comprising:

a first interface (such as *Hardware Model B*) operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry; and a second interface (such as Hardware Model C) operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (such as *Signal Bus 1 and Signal Bus 2 having bi-directional for input/output from first circuitry such as Emulator B and second circuitry such as Emulator C as shown in Fig. 3*).

As per Claim 6:

Hill discloses a method for verifying a plurality of systems on chip (See: Col. 5 lines 3-8; Fig. 1), the method comprising:

verifying a first system on a chip with a first portion of a hardware emulator; and verifying a second system on another chip with a second portion of the hardware emulator while verifying the first system on chip (See: Abstract lines 5-8, Col. 5 lines 24-26 and 31-33; Fig. 1);

configuring the first portion of the hardware emulator to realize the first system on chip; and configuring the second portion of the hardware emulator to realize the second system on chip (See: Col. 8 lines 35-37).

As per Claim 7:

Canceled.

As per Claim 8:

Hill discloses configuring the first portion of the hardware emulator comprises receiving a portion of a top wrapper describing the first system on chip and wherein configuring the second portion of the hardware emulator comprises receiving another portion of a top wrapper describing the second system on another chip (See: Col. 3 lines 55-59, Col. 5 lines 17-23).

As per Claim 9:

Hill discloses the method of claim 6, wherein verifying the first system on chip further comprises: providing inputs to the first portion; and receiving outputs from the first portion (See: Col. 6 lines 5-8).

As per Claim 10:

Hill discloses a computer readable medium for configuring a hardware emulator, said computer readable medium storing a top wrapper (such as *a program that is written in hardware description languages such as* ...; See: Col. 5 lines 17-23) comprising:

a first design structure for describing a first system on chip (such as *Hardware Model B*; See: Col. 3 lines 55-61; Fig. 1); and

a second design structure fro describing a second system on another chip (such as *Hardware Model C*; See: Col. 3 lines 55-61; Fig. 1).

11. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by US Publication No. US 2002/0129334 A1 issued to Dane et al.

As per Claim 11:

Dane discloses a computer readable medium for configuring a hardware emulator, said computer readable medium storing a data structure, the data structure (See: Fig. 5A) comprising:

a first design structure for describing a first system on chip (such as *Component Module 1*; See: Fig.5A lines 517-523e) wherein the first design structure further comprises:

a first ports declaration for describing ports associated with the first system on chip (See: [0055] lines 21-30; Fig. 6A Block 650);

a first design information for describing at least a portion of the first system on chip (See: [0044]); and

an end of first design structure indicator, for indicating the end of the first design structure (See: [0055] lines 37-40); and

a second design structure for describing the second system on chip (such as *Component Module 2)*, wherein the second design structure further comprises:

a second port declaration for describing ports associated with the second system on another chip (See: [0056] lines 1-7; Fig. 6A and 6B Blocks 660, 670, and 675);

a second design information for describing at least a portion of the first system on another chip (See: [0044]); and

an end of second design structure indicator, for indicating the end of the second design indicator (See: the second flow chart of Fig. 6B); and

the second design structure immediately following the end of first design structure indicator (See: Fig. 5A lines 523 –525 that shows the end of Design structure of Component Module 1 and following the Design structure of Component Module 2).

Conclusion

12. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

13. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communications

14. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kamini S. Shah can be reached at (571) 272-2279. The official fax number is (571) 273-8300. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER